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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TSAI, SHENG JEN	
ART UNIT	**PAPER NUMBER**
2186	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/511,877	HOLMBERG ET AL.	
	Examiner	Art Unit	
	Sheng-Jen Tsai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 14-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 14-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/19/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-22 are presented for examination in this application (10,511,877) filed on October 19, 2004.

Claim Objections

2. The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

It is noted that the numbering of the claims indicates the absence of **claim 13**. In order to maintain the current numbering, the Examiner treats claim 13 as being **cancelled**.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 14 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 14 recites "the computer system according to **claim 13**, ..." However, claim 13 no longer exists, rendering claim 14 indefinite.

For the following claim analysis, the Examiner interprets claim 14 as "the computer system according to **claim 12**, ..."

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-5, 7-12 and 14-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Wollan et al. (US 5,854,939).

It is noted that, in the following claim analysis, those elements recited by the claims are presented in **bold** font.

As to claim 1, Wollan et al. disclose **a computer system** [Eight-Bit Microcontroller Having a RISC Architecture (title); figure 1] **comprising**:

a special-purpose register file [the Register File, figure 1; figures 2A~2C, 100] **adapted for holding memory address calculation information received from memory** [The register file includes a plurality of eight-bit registers. Certain of the registers in the register file can be combined to provide logical 16-bit registers. A logical 16-bit register provides efficient address calculation and is used as an indirect address pointer into data memory and program memory (column 2, lines 16-22); the program memory, figure 1; the SRAM, figure 1], **said special-purpose register file having at least one dedicated interface for allowing efficient transfer of memory address calculation information in relation to said special-purpose register file** [figure 1 shows a dedicated interface between the program memory and the register

file via the instruction register; figure 1 also shows another dedicated interface between the SRAM and the register file; column 3, lines 58-65];

means for determining a memory address in response to memory address calculation information received from said special-purpose register file, thus enabling a corresponding memory access [The register file further includes means for combining a pair of registers to provide a logical sixteen-bit register for indirect addressing. The dedicated ALU is a sixteen-bit ALU which provides certain arithmetic functions for the register pair, thus alleviating the computational burdens that would otherwise be imposed on the general purpose eight-bit ALU (abstract)].

As to claim 2, Wollan et al. teach that **the computer system according to claim 1, further comprising means for effectuating a memory access based on the determined memory address** [The register file further includes means for combining a pair of registers to provide a logical sixteen-bit register for indirect addressing. The dedicated ALU is a sixteen-bit ALU which provides certain arithmetic functions for the register pair, thus alleviating the computational burdens that would otherwise be imposed on the general purpose eight-bit ALU (abstract)].

As to claim 3, Wollan et al. teach that **the computer system according to claim 1, wherein said at least one dedicated interface comprises a dedicated interface between said special-purpose register file and memory** [figure 1 shows a dedicated interface between the program memory and the register file via the instruction register; figure 1 also shows another dedicated interface between the SRAM and the register file; column 3, lines 58-65].

As to claim 4, Wollan et al. teach that **the computer system according to claim 1, wherein said at least one dedicated interface comprises a dedicated interface between said special-purpose register file and said means for determining a memory address** [figure 2A shows a dedicated interface between the register file (100) and the ALU-2, which is the corresponding means for determining a memory address].

As to claim 5, Wollan et al. teach that **the computer system according to claim 1, wherein said at least one dedicated interface includes a dedicated data path adapted in width to said memory address calculation information** [The register file includes a plurality of eight-bit registers. Certain of the registers in the register file can be combined to provide logical 16-bit registers. A logical 16-bit register provides efficient address calculation and is used as an indirect address pointer into data memory and program memory (column 2, lines 16-22); A further extension of the logical 16-bit register provided in the register file is the use of an 8-bit RAM paging register. The eight bits of the RAM paging register are logically concatenated with the sixteen bits of the logical 16-bit register to provide a logical 24-bit address (column 2, lines 39-43)].

As to claim 7, Wollan et al. teach that **the computer system according to claim 1, wherein said means for determining a memory address comprises at least one functional processor unit** [the ALU-1 and ALU-2 as shown in figures 2A~2C].

As to claim 8, Wollan et al. teach that **the computer system according to claim 7, wherein a forwarding data path is arranged from an output bus associated**

with said at least one functional processor unit to an input bus associated with said at least one functional processor unit [figure 2A shows that the output from the ALU-1 unit is connected via an 8-bit bus (12) and feedback into the input side of the ALU unit].

As to claim 9, Wollan et al. teach that **the computer system according to claim 1, wherein said means for determining a memory address is operable for executing special-purpose instructions in order to determine said memory address** [columns 8~11 show a plurality of special instructions all related to the determining of memory address].

As to claim 10, Wollan et al. teach that **the computer system according to claim 1, further comprising means for executing special-purpose load instructions in order to load said memory address** calculation information from said memory to said special-purpose register file [For the load instruction, the DATA8 IN control signal operates the lo-byte data-in latch 126 to latch in the data referenced by the 16 bit register, which is then loaded into the 8 bit register selected by the R0-R31 SELECT control signal (column 14, lines 47-51)].

As to claim 11, Wollan et al. teach that **the computer system according to claim 10, wherein said means for executing special-purpose load instructions comprises at least one functional processor unit** [For the store instruction, the DATA8 OUT control signal operates the lo-byte data-out latch 122 to output the contents of the 8 bit register selected by the R0-R31 SELECT control signal, which is

then stored into the memory location pointed to by the 16 bit register (column 14, lines 51-55)].

As to claim 12, Wollan et al. teach that **the computer system according to claim 11, wherein a forwarding data path is arranged from said memory to an input wherein said memory address calculation information is in the form of implicit memory access information** [figure 1 shows a dedicated interface between the program memory and the register file via the instruction register, one filed of the instruction register may contain implicit memory access information such as indirect addressing mode as opposed to direct addressing mode; columns 8~11 show a plurality of special instructions all related to the determining of memory address].

As to claim 14, Wollan et al. teach that **the computer system according to claim 12, wherein said implicit memory access information includes memory address translation information** [figure 1 shows a dedicated interface between the program memory and the register file via the instruction register, one filed of the instruction register may contain implicit memory access information such as indirect addressing mode as opposed to direct addressing mode; columns 8~11 show a plurality of special instructions all related to the determining of memory address].

As to claim 17, refer to "As to claim 1" presented earlier in this Office Action.

As to claim 18, refer to "As to claim 2" presented earlier in this Office Action.

As to claim 19, refer to "As to claim 3" presented earlier in this Office Action.

As to claim 20, refer to "As to claim 4" presented earlier in this Office Action.

As to claim 21, refer to "As to claim 5" presented earlier in this Office Action.

7. Claims 1, 6, 15, 17 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Aikawa et al. (US 5,371,865).

As to claim 1, Aikawa et al. disclose **a computer system** [Computer with Main Memory and Cache memory for Employing Array Data Pre-Load operation Utilizing base-Address and Offset operand (title); figures 4A and 4B] **comprising**:
a special-purpose register file [the Register File, figure 4B, 53] **adapted for holding memory address calculation information received from memory** ["$25" and "($4)" are supplied to register file 53 through line 55. The base address stored in register "$4" is read from register file 53 (column 7, lines 1-3)], **said special-purpose register file having at least one dedicated interface for allowing efficient transfer of memory address calculation information in relation to said special-purpose register file** [figure 4B shows a dedicated interface (50) between the data memory (32) and the register file (53)];
means for determining a memory address in response to memory address calculation information received from said special-purpose register file, thus enabling a corresponding memory access [The corresponding means is the ALU (figure 4B, 57); At the same time, ALU 57 adds the base address, which is received through line 59, to offset "64" which is received through selector 58. Then ALU 57 stores the addition result, which is a new base address, in register "$3" of register file 53 through line 60 (column 7, lines 13-17)].

As to claim 6, Aikawa et al. teach that **the computer system according to claim 1, wherein said memory comprises a dedicated cache adapted for said**

memory address calculation information [A computer having a main memory for storing a plurality of data, a cache memory for temporarily storing a portion of the plurality of data, a processor for accessing data stored in the cache memory and processing the data according to instructions. The processor has an access instruction combined with a preload instruction, and an access instruction only for accessing data, and includes indicator circuitry for indicating a preload condition to the cache memory when the processor accesses data from the cache memory according to the access instruction combined with the preload instruction. The cache memory preloads data to be accessed next by the processor from the main memory when the processor indicates the preload condition (abstract)].

As to claim 15, Aikawa et al. disclose **a computer system** [Computer with Main Memory and Cache memory for Employing Array Data Pre-Load operation Utilizing base-Address and Offset operand (title); figures 4A and 4B] **comprising**:

a dedicated cache adapted for holding memory access information [A computer having a main memory for storing a plurality of data, a cache memory for temporarily storing a portion of the plurality of data, a processor for accessing data stored in the cache memory and processing the data according to instructions. The processor has an access instruction combined with a preload instruction, and an access instruction only for accessing data, and includes indicator circuitry for indicating a preload condition to the cache memory when the processor accesses data from the cache memory according to the access instruction combined with the preload instruction. The

cache memory preloads data to be accessed next by the processor from the main memory when the processor indicates the preload condition (abstract)];

a special-purpose register file [the Register File, figure 4B, 53] **adapted for holding memory access information received from said dedicated cache over a first dedicated interface** ["$25" and "($4)" are supplied to register file 53 through line 55. The base address stored in register "$4" is read from register file 53 (column 7, lines 1-3); figure 4B shows a dedicated interface (50) between the data memory (32) and the register file (53)];

means for determining a memory address in response to memory access information received from said special-purpose register file over a second dedicated interface [The corresponding means is the ALU (figure 4B, 57); At the same time, ALU 57 adds the base address, which is received through line 59, to offset "64" which is received through selector 58. Then ALU 57 stores the addition result, which is a new base address, in register "$3" of register file 53 through line 60 (column 7, lines 13-17)]; **and**

means for effectuating a corresponding memory access based on the determined memory address [Therefore, the data control section 34 sends the pre-load address to main memory 20. Then, data corresponding to the pre-load address are transferred from main memory 20 to data memory section 32 (column 7, lines 24-27)].

As to claim 17, refer to “As to claim 1” and “As to claim 15” presented earlier in this Office Action.

As to claim 22, refer to "As to claim 6" presented earlier in this Office Action.

8. ***Related Prior Art of Record***

The following list of prior art is considered to be pertinent to applicant's invention, but not relied upon for claim analysis in this Office Action.

- Baror et al., (US 4,926,323), "Streamlined Instruction processor."
- Henry et al., (US 6,862,670), "Tagged Address Stack and Microprocessor Using Same."

Conclusion

9. Claims 1-12 and 14-22 are rejected as explained above.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheng-Jen Tsai whose telephone number is 571-272-4244. The examiner can normally be reached on 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sheng-Jen Tsai
Examiner
Art Unit 2186

December 14, 2006

PIERRE BATAILLE
PRIMARY EXAMINER
1/11/07